ABSTRACT

The present inventions is a method of trench formation within a dielectric layer, comprising, first, etching a via within the dielectric layer. After the via is etched, an organic plug is used to fill a portion of the via. After the desired amount of organic plug has been etched from the via, a trench is etched with a first gas mixture to a first depth, and a second gas mixture is used to further etch the trench to the final desired trench depth. Preferably, the method is used for low-k dielectrics that do not have an intermediate etch stop layer. Additionally, it is preferable that the first gas mixture is a polymeric gas mixture and the second gas mixture is a non-polymeric gas mixture. As a result of using this method, an interconnect structure for a low-k dielectric without an intermediate etch stop layer having a trench with trench edges that are substantially orthogonal and a via with via edges that are substantially orthogonal is generated.